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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/841,799	04/24/2001	Ricky Keang-Po Ho	0259668 ST-005	6808

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EXAMINER	
RIZK, SAMIR WADIE	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 06/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/841,799	HO ET AL.	
	Examiner	Art Unit	
	Sam Rizk	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *27-42* is/are allowed.

6)☒ Claim(s) *1-3,7,8 and 14-26* is/are rejected.

7)☒ Claim(s) *4-6,9-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/2[illegible]/2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTIONS

- Claims 1-42 have been submitted for examination
- Claims 1-3,7,8,14-26 have been rejected
- Claims 4-6,9-13 are objected to.
- Claims 27-42 are allowed

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-42 are rejected under 35 U.S.C. 102(e) as being anticipated by Kuwata US patent no. 6595707 (Hereinafter Kuwata).

2. In regard to claim 1, Yonenaga teaches:

   - A circuit to calculate the cumulative parity of a binary number sequence, comprising:
   - an array of functional modules, the modules aligned to form columns and rows within the array, the array configured to receive the binary number sequence at a first column of the modules and to produce the cumulative parity as output at a last column of the modules, each of the modules being one of:

(Note: Figures 11 and 12 in Kuwata)

- a parity module configured to receive certain input bits from one of the binary number sequence and a previous column and to calculate the parity of the certain input bits; and

(Note: Figure 11, reference signs (22-1)-(22-N) in Kuwata)

- a delay module configured to receive other input bits from one of the binary number sequence and a previous column and to delay the other input bits.

(Note: Figure 12, reference sign (63) in Kuwata)

3. In regard to claim 2, Kuwata teaches:

- The circuit of claim 1, wherein calculations within the array proceed from the first column to the last column and the array includes one more column than row.

(Note: Claim 10 in Kuwata)

4. In regard to claim 3, Kuwata teaches:

- The circuit of claim 1, wherein the parity modules form the last column of the modules:

(Note: Figure 12, reference sign (64) in Kuwata)

5. In regard to claim 7, Kuwata teaches:

- The circuit of claim 1, wherein any delay modules within the same row of the array, have the same number of inputs and outputs.

(Note; Figure 12, reference sign (63) in Kuwata)

6. In regard to claim 8, Kuwata teaches:

- The circuit of claim 1, wherein within a given row of the array, the number of parallel inputs and outputs of any parity module is equal to the number of inputs and outputs of any delay module.

(Note; Figure 12, in Kuwata)

7. In regard to claim 14, Kuwata teaches;

- The circuit of claim 1, wherein a number of inputs of the party module exceed the a number of outputs of the parity module by one, wherein output bits are provided from the outputs of the parity module, and wherein the first output provides a first output bit that is the parity of the certain input bits received at the first two inputs, the second output provides a second output bit that is the parity of the certain input bits received at the first three inputs, and the ith output provides ala ith output bit that is the parity of the certain input bits received at the first i +1 outputs.

(Note: Figure 12, reference sign (64) in Kuwata)

8. In regard to claim 15, Kuwata teaches:

- The circuit of claim 1, wherein a first number of other input bits received by a delay module in one row of the array is not equivalent to a second number of other input bits received by a delay module in another row of the array.

(Note: Figures (5-6) and col.9, lines (62-67) through col. 10, lines (1-12) in Kuwata)

9. In regard to claim 16, Kuwata teaches:

- The circuit of claim 1, wherein a first number of certain input bits received by a parity module in one row of the array is not equivalent to a second number of certain input bits received by a parity module in another row of the array.

(Note: Figures (5-6) and col.9, lines (62-67) through col. 10, lines (1-12) in Kuwata)

10. In regard to claim 17, Kuwata teaches:

- The circuit of claim 1, further comprising: at least one circuit element to align the timing and the delay of logic gates within the circuit and the array.

(Note: Figure 7, reference sign (INV) in Kuwata)

11. In regard to claim 18, Kuwata teaches:

- The circuit of claim 1, wherein each delay module comprises at least one D-type flip flop.

(Note; Figure 7, reference sign ((17) in Kuwata)

12. In regard to claim 19, Kuwata teaches:

- The circuit of claim 1, wherein each delay module comprises a bank of D-type flip-flops.

(Note: Figure 12, reference sign (63) in Kuwata0

13. In regard to claim 20, Kuwata teaches:

- The circuit of claim 1, wherein each delay module comprises a component having a triggered delay for one clock cycle.

(Note: Figure 11, reference sign (62) in Kuwata)

14. In regard to claim 21, Kuwata teaches:

- The circuit of claim 1, wherein each parity module comprises at least one D-type flip-flop.

(Note: Figure 10, reference sign (17) in Kuwata)

15. In regard to claim 22, Kuwata teaches:

- The circuit of claim 1, wherein, each parity module comprises at least one XOR gate and at least one D-type flip-flop.

(Note: Figure 10, reference signs (15 & 17) in Kuwata)

16. In regard to claim 23, Kuwata teaches:

- The circuit of claim 1, wherein each parity module composes a ladder of XOR gates and a bank of D-type flip-flops.

(Note: Figure 10, reference signs (15 & 17) in Kuwata)

17. In regard to claim 24, Kuwata teaches:

- The circuit of claim 1, wherein each parity module comprises a ladder of XOR gates, a bank of XOR gates, and a bank of D-type flip-flops.

(Note: Figure 10, reference signs (15 & 17) in Kuwata)

18. In regard to claim 25, Kuwata teaches:

- The circuit of claim 1, wherein the circuit is used as the differential precoder before a time-division multiplexer for a duobinary transmitter in an optical communication system.

(Note: Yoneyama et al., Differential precoder IC modules for over 20-Gbps Duobinary Transmission Systems" IEE MIT-S international Microwave Symposium, 1999. incorporated by reference in Kuwata0

19. In regard to claim 26, Kuwata teaches:

- The circuit of claim 1, wherein the circuit is used as the differential precoder for duobinary transmission, the differential precoder operating in parallel and having at least two parallel inputs.

(Note: Yoneyama et al.,: Differential precoder IC modules for over 20-Gbps Duobinary Transmission Systems" IEE MIT-S international Microwave Symposium, 1999. incorporated by reference in Kuwata0

Allowable Subject Matter

20. Claims 4,5,6,9-13, 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

21. Claims 33-42 are allowed.

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

21. In regard to claim 4, the prior Art of record, in particular Kuwata teaches all the limitations in claim 3.

However, the prior art do not teach, suggest, or otherwise render obvious:

The circuit of claim 3, wherein the first column of modules to the second to last Column of modules forms an inner array having an equivalent number of rows and columns of modules, wherein within the inner array of modules the parity modules **form a diagonal of the inner array from a first row to a last row and the delay modules are the remaining modules within the inner array.**

22. Claims (5,6,9-13) depend from claims 1.

23. Claim 27 cite similar language to claim 1:

- A circuit to calculate the cumulative parity of a binary limber sequence, comprising:
- an array of delay elements, the delay elements aligned to form M + 1 columns and M rows within the array, where M represents a number of parallel input bit values, and wherein the array is configured to receive the binary number sequence at the first column of the delay elements and to produce the cumulative parity as output at the (M+1)th column of the delay elements, the array comprising:
- **diagonal delay elements forming a diagonal of an M column by M row inner array of the array, from the first row and the first column to the Mth row and the Mth column of the array; non-diagonal delay elements, wherein the non-diagonal delay**

elements are the remaining delay elements within the inner array; and the (M+1)th column delay elements;

- diagonal gate elements located from the second row through the Mth rows of the array to calculate parity information, the diagonal gate elements each having a diagonal gate output connected to a diagonal delay input of the corresponding diagonal delay element in the same row and the next column of the array, a first diagonal gate input connected to a diagonal delay output of the corresponding diagonal delay element in the prior row and the previous column of the array, and a second diagonal gate input connected to a non-diagonal delay output of the corresponding non-diagonal delay element in the same row and the previous column of the array; and
- column gate elements located from the first row to the Mth row of the array and between the Mth column and the (M+1)th column of the array, the column gate elements each having a column gate output connected to a column delay input of the corresponding (M+1)th column delay element in the same row of the array, the column gate elements used to pass the parity information from the diagonal and non-diagonal outputs of respective diagonal and non-diagonal delay elements in prior columns of the array to the (M+1)th column delay elements.

24. Claims 28-32 depend from claim 27.

25. Claim 33 cite similar language to claim 1:

- **A method of using an array of M(M+1) modules to calculate the cumulative parity of a binary number sequence, the array comprising M rows of M+1 modules and M+1 columns of M modules, the method comprising:**
- within a first clock cycle T:
- calculating the cumulative parity of a first input group of n input bit values and a first initial parity input value at the first row first column module;
- delaying a second input group of n input bit values at the second row first column module; and
- delaying an Mth input group of n input bit values at the Mth row first column module;
- within a second clock cycle 2T:
- delaying the cumulative parity of the first input group at the first row second column module;
- calculating the cumulative parity of the second input group and a second initial parity input bit value at the second row second column module; and
- delaying the Mth input group at the Mth row second column module; within an Mth clock cycle MT:

- delaying the cumulative parity of the first input group at the first row Mth column module;
- delaying the cumulative parity of the second input group at the second row Mth column module; and
- calculating the cumulative parity of the Mth input group and an Mth initial parity input bit value at the Mth row Mth column module; and
- within an (M+1)th clock cycle (M+1)T:
- calculating a first output group of n output bit values at the first row (M+1)th column module;
- calculating a second output group of n output bit values at the second row (M+1)th column module; and calculating an Mth output group of n output bit values at the Mth row (M+1)th column module.

26. Claims 34-40 depend from claim 33.

27. claims 41 and 44 cite similar language to claim 33.

Conclusion

24. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Yonenaga et al US patent no. 6934308 teaches precoding circuit and precoding multiplexing circuit for realizing very high transmission rate in optical fiber communication
- Gurusami et al US patent no. 6643371 teaches increased transmission capacity for fiber optic link.

- Ono et US patent no. 6388786 teaches method for generating duobinary signal and optical transmitter.
- Mizuhara US patent no. 6522438 teaches high-speed optical duobinary modulation scheme.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Rizk whose telephone number is (571) 272-8191. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronics Business Center (EBC) at 866-217-9197 (toll-free)

Sam Rizk, MSEE, ABD

Examiner

ART UNIT 2133

5/23/06

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